ABSTRACT OF THE DISCLOSURE

Device and method for digitally generating equidistant synchronous frequency-multiplied clock pulses.

Uniform distribution of a correction determined by a PLL over the subordinate clock signals is undertaken by dividing a phase-regulated value by the number of subordinate clock signals. Division by way of successive addition is performed such that time conflicts with subordinate clock signals generated in real time are successfully avoided despite the required time duration of such a division. The synchronicity can be further raised by also uniformly distributing a division remainder. A particularly effective implementation of this division employs subsequent rounding for real time use.